Remarks

In the official action the Examiner rejects claims 1-8 as allegedly being fully anticipated by US Patent No. 5,384,475 to Yahata. This ground for rejection is respectfully traversed.

In the analysis provided by the Examiner, the Examiner makes reference to "spaced-apart doped regions" as well as "a first doped region" and "a second doped region". However, this language does not comport with the language of the claims. For example, claim 1 and the claims which depend therefrom refer to "spaced-apart implanted regions", "a first implanted region" and "a second implanted region". Claim 5 and the claims which depend therefrom refer to "spaced-apart implanted regions" and "selected implant regions". The difference is important because the Examiner tries to read "a second implanted region" (using the language of claim 1) on region 14 of Yahata. However, region 14 is clearly not a implanted region, but rather is formed epitaxially. This difference is of importance to Yahata since Yahata teaches that his diffused wiring regions are quite deep compared to their thickness. See the passages towards the bottom of column 4 of Yahata. Moreover, it is believed that a person skilled in the art would want to keep the diffused wiring regions away from the channel regions under the gates. See, for example, Figure 5E-I. That can be easily accomplished by following the teaching of Yahata and thus use epitaxial growth. It is clear that Yahata does not meet the limitations of claims 1-8. Therefore the Examiner's rejection under 35 U.S.C. 102 is improper and the Examiner is respectfully requested to withdraw the rejection.

Claims 15, 18 and 19 have each been amended to more clearly differentiate those claims from Yahata.

Yahata teaches a semiconductor device and a method of making same wherein the device is an EPROM. The EPROM has a very regular pattern as would be expected of memory devices. As such, a reverse engineer would not be fooled by Yahata's device even though Yahata does bury some of his conductors in order to make the

device smaller.

Since Yahata has very regular patterns, he tends to connect up the drains, for example, of the devices in parallel using his buried interconnect scheme.

Compare Yahata with the embodiment of Applicant's invention shown in Figure 5 wherein four transistor elements are shown and wherein the drains and sources of neighboring transistors are connected together by a buried interconnect scheme. Note how drains can be connected to sources and that the pattern is anything but the sort of regular pattern that a person of ordinary skill in the art would see in a memory device such as Yahata's.

The preamble of claim 15 has been amended to indicate that the integrated circuit or device has "a plurality of spaced-apart regions arranged as transistors, said two spaced-apart doped regions each forming an active region in different ones of said transistors and each providing a different transistor function with respect to the transistor in which it forms an active region..." In Yahata, it is believed that the transistors are all being wired up in parallel in a very regular fashion and when the buried interconnect is used, it is used to connect up the neighboring transistors so that the active areas which have an identical function with respect to each transistor are interconnected. As such, Yahata teaches away from claim 15 as presently amended.

Claim 19, as amended, recited that "each buried elongate conducting channel" has "a major axis which is arranged in a non-parallel relationship to each other elongate conducting channel of said plurality of buried elongate conducting channels..." Note that in the embodiment of Figure 5, the two elongate buried conducting channels are disposed at right angles to each other. In Yahata, on the other hand, given its regular structure, the conducting channels are all parallel to one another. Yahata teaches away from claim 19 as amended.

Claim 18 has been amended to indicate that "the integrated circuit or device" has "a plurality of spaced-apart regions arranged as transistors, said two spaced-apart

doped regions each forming an active region in different ones of said transistors" and that the at least one additional spaced-apart region forms "an active region in yet another different one of said transistors..." The quoted language clearly distinguishes claim 18 from Yahata since the "at least one additional spaced-apart region" to which the Examiner pointed, namely region 9, 10b are not "in yet another different one of said transistors" as required by claim 18.

Reconsideration of this application as amended is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents POB 1450, Alexandria, VA 22313-1450 on

June 24, 2003

(Date of Deposit)

Corinda Humphrey

(Name of Person Signing)

Corinda Humphrey

(Signature)

June 24, 2003

(Date)

Respectfully submitted,

Richard P. Berg
Attorney for Applicants
Reg. No.28,145
LADAS & PARRY
5670 Wilshire Boulevard, Suite 2100
Los Angeles, California 90036
(323) 934-2300